



Approval



TO : Asus

DATE : May. 26, 2011

SAMSUNG TFT-LCD**MODEL NO : LTN156HT01-201**

NOTE : Extension code [-2]
→ LTN156HT01-2
Surface type [Anti-Glare]

Any modification of Spec is not allowed without SEC's permission

APPROVED BY : _____

PREPARED BY : _____

Stan Kim**Application Engineer Group****SAMSUNG ELECTRONICS CO., LTD.****Samsung Secret**

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REVISION HISTORY

Approval

Date	Revision No.	Page	Summary
May, 26. 2011	A00	All	The Approval specification of LTN156HT01-2 was issued first

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GENERAL DESCRIPTION

DESCRIPTION

LTN156HT01-201 is a color active matrix TFT (Thin Film Transistor) liquid crystal display (LCD) that uses amorphous silicon TFT as switching devices. This model is composed of a TFT LCD panel, a driver circuit and a backlight system. The resolution of a 15.6" contains 1920 x 1080 pixels and can display up to 262,144 colors. 6 O'clock direction is the Optimum viewing angle.

FEATURES

- 1920 x 1080 pixels resolution (16:9)
- Fast Response Time
- Low power consumption
- LED BLU Structure
- DE (Data enable) only mode
- 3.3V LVDS Interface
- On board EDID chip
- RoHS compliance
- PVC free compliance
- BFR free compliance
- As free compliance

APPLICATIONS

- Notebook PC
- If the usage of this product is not for PC application, but for others, please contact SEC

GENERAL INFORMATION

Item	Specification	Unit	Note
Display area	344.16 (H) x 193.59 (V) (15.6"diagonal)	mm	
Driver element	a-Si TFT active matrix		
Display colors	262,144		
Number of pixel	1920 x 1080	pixel	16 : 9
Pixel arrangement	RGB vertical stripe		
Pixel pitch	0.179 (H) x 0.179 (V) (TYP.)	mm	
Display Mode	Normally white		
Surface treatment	Haze 25%, Hardness 3H		Anti-Glare

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Mechanical Information

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal (H)	358.8	359.3	359.8	mm	
	Vertical (V)	209.0	209.5	210.0	mm	
	Depth (D)	-	-	5.8	mm	(1)
Weight		-	-	510	g	

Note (1) Measurement condition of outline dimension

- . Equipment : Vernier Calipers
- . Push Force : 500g .f (minimum)

1. ABSOLUTE MAXIMUM RATINGS

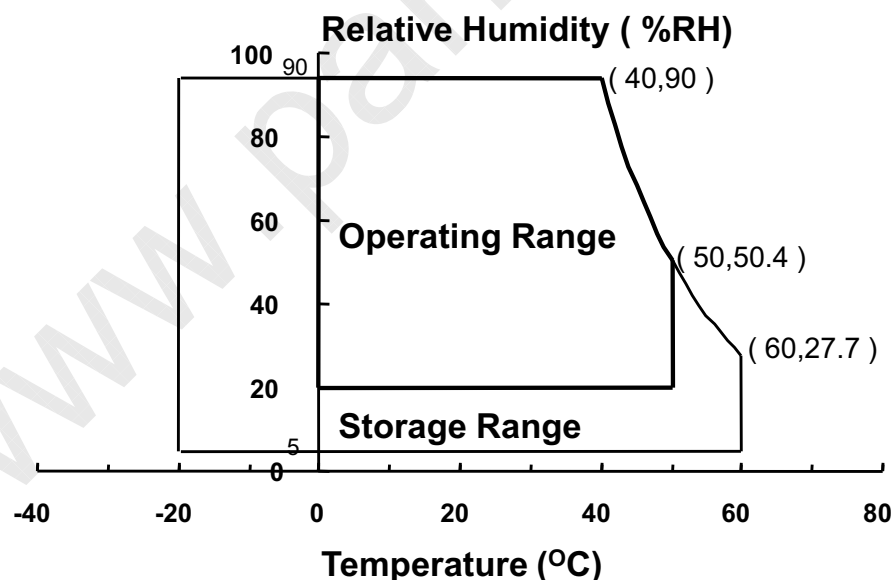
1.1 ENVIRONMENTAL ABSOLUTE RATINGS

Item	Symbol	Min.	Max.	Unit	Note
Storage temperate	TSTG	-20	60	°C	(1)
Operating temperate (Temperature of glass surface)	TOPR	0	50	°C	(1)
Shock (non-operating)	Snop	-	240	G	(2),(4)
Vibration (non-operating)	Vnop	-	2.41	G	(3),(4)

Note (1) Temperature and relative humidity range are shown in the figure below.

95 % RH Max. ($40^{\circ}\text{C} \geq T_a$)

Maximum wet - bulb temperature at 39°C or less. ($T_a > 40^{\circ}\text{C}$) No condensation



(2) 2ms, half sine wave, one time for $\pm X$, $\pm Y$, $\pm Z$.

(3) 5 - 500 Hz, random vibration, 30min for X, Y, Z.

(4) At testing Vibration and Shock, the fixture in holding the Module to be tested have to be hard and rigid enough so that the Module would not be twisted or bent by the fixture.

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1.2 ELECTRICAL ABSOLUTE RATINGS

(1) TFT LCD MODULE

V_{DD} = 3.3V, V_{SS} = GND = 0V

Item	Symbol	Min.	Max.	Unit	Note
Power Supply Voltage	V _{DD}	V _{DD} - 0.3	V _{DD} + 0.3	V	(1)
Logic Input Voltage	V _{DD}	V _{DD} - 0.3	V _{DD} + 0.3	V	(1)

Note (1) Within Ta (25 ± 2 °C)

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2. OPTICAL CHARACTERISTICS

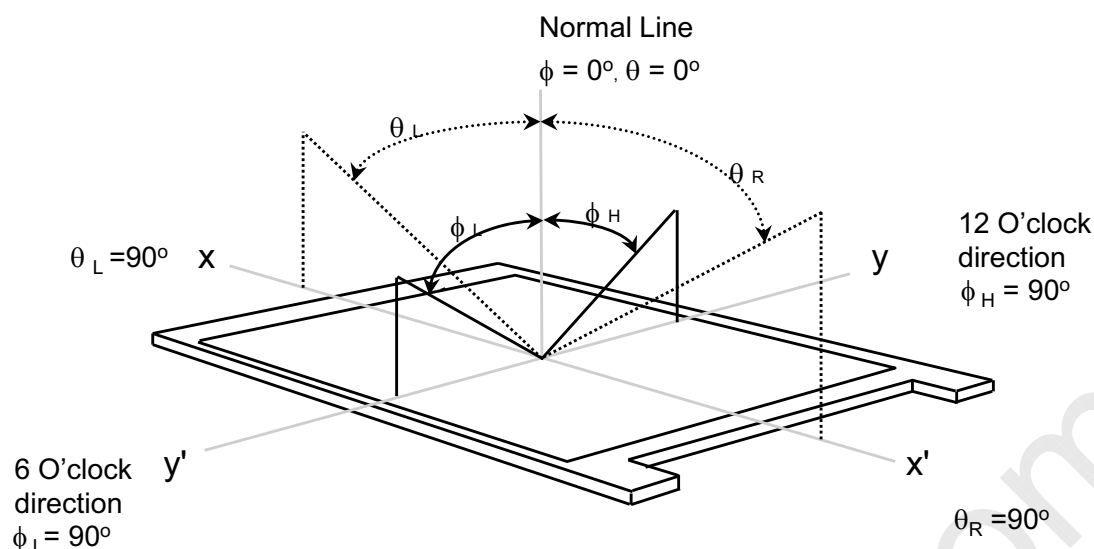
The following items are measured under stable conditions. The optical characteristics should be measured in a dark room or equivalent state with the methods shown in Note (5).
 Measuring equipment : TOPCON SR-3

* Ta = 25 ± 2 °C, VDD=3.3V, fv= 60Hz, fDCLK = 138.65 MHz, IL = 24 mA

Item		Symbol	Condition	Min.	Typ.	Max	Unit	Note
Contrast Ratio (5 Points)		CR	Normal Viewing Angle $\phi = 0$ $\theta = 0$	500	-	-	-	(1), (2), (5)
Response Time at Ta (Rising + Falling)		T _{RT}		-	16	25	msec	(1), (3)
Average Luminance of White (5 Points)		Y _{L,AVE}		250	300	-	cd/m ²	I _L =24 mA (1), (4)
Color Chromaticity (CIE)	Red	R _X		Typ -0.03	0.613	Typ -0.03	-	
		R _Y			0.361			
	Green	G _X			0.338			
		G _Y			0.603			
	Blue	B _X			0.155			
		B _Y			0.104			
	White	W _X			0.313			
		W _Y	0.329					
Viewing Angle	Hor.	θ_L	CR ≥ 10	50	-	-	Degrees	(1), (5) SR-3
		θ_R		50	-	-		
	Ver.	ϕ_H		40	-	-		
		ϕ_L		40	-	-		
Color Gamut				-	60	-	%	
13 Points White Variation		δ_L		-	-	1.7	-	(6)

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Note 1) Definition of Viewing Angle : Viewing angle range($10 \leq C/R$)

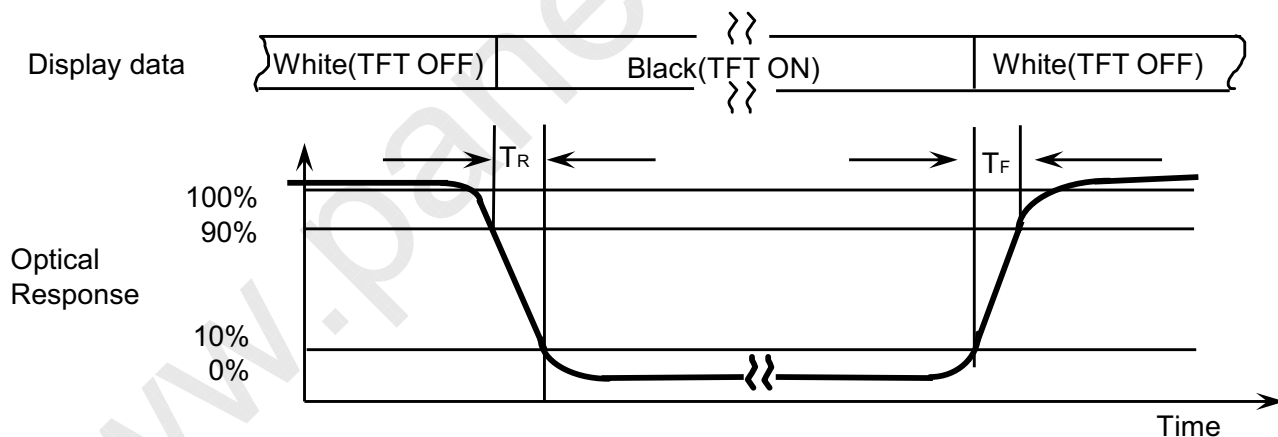


Note 2) Definition of Contrast Ratio (CR) : Ratio of gray max (Gmax) ,gray min (Gmin) at 5 points (33, 55, 77, 37, 73)

$$CR = \frac{CR(33) + CR(55) + CR(77) + CR(37) + CR(73)}{5}$$

Points : 33, 55, 77, 37, 73 at the figure of Note (6).

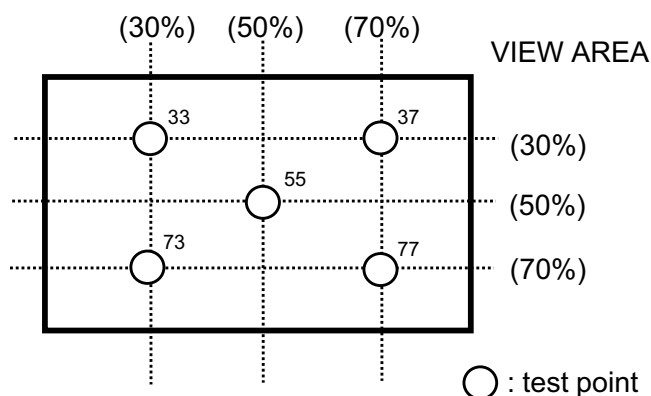
Note 3) Definition of Response time :



Note 4) Definition of Average Luminance of White : measure the luminance of white at 5 points.

Average Luminance of White ($Y_{L,AVE}$)

$$Y_{L,AVE} = \frac{Y_{L33} + Y_{L55} + Y_{L77} + Y_{L37} + Y_{L73}}{5}$$

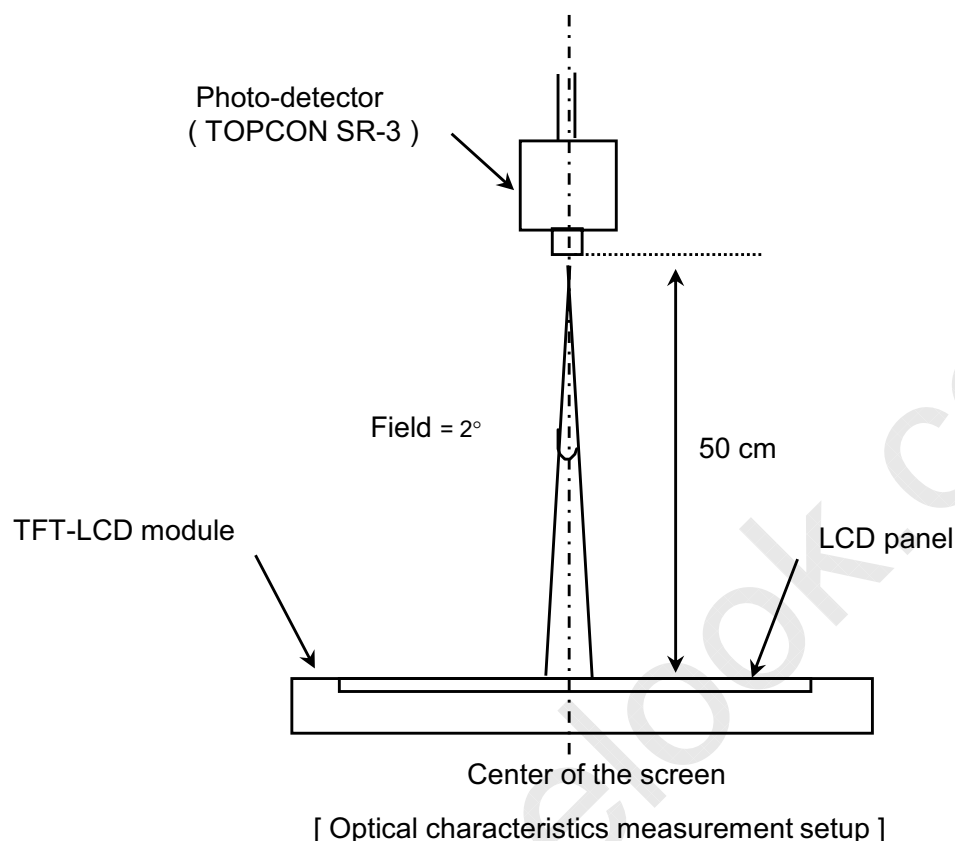


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Note 5) After stabilizing and leaving the panel alone at a given temperature for 30 min , the measurement should be executed. Measurement should be executed in a stable, windless, and dark room. 30 min after lighting the backlight. This should be measured in the center of screen.

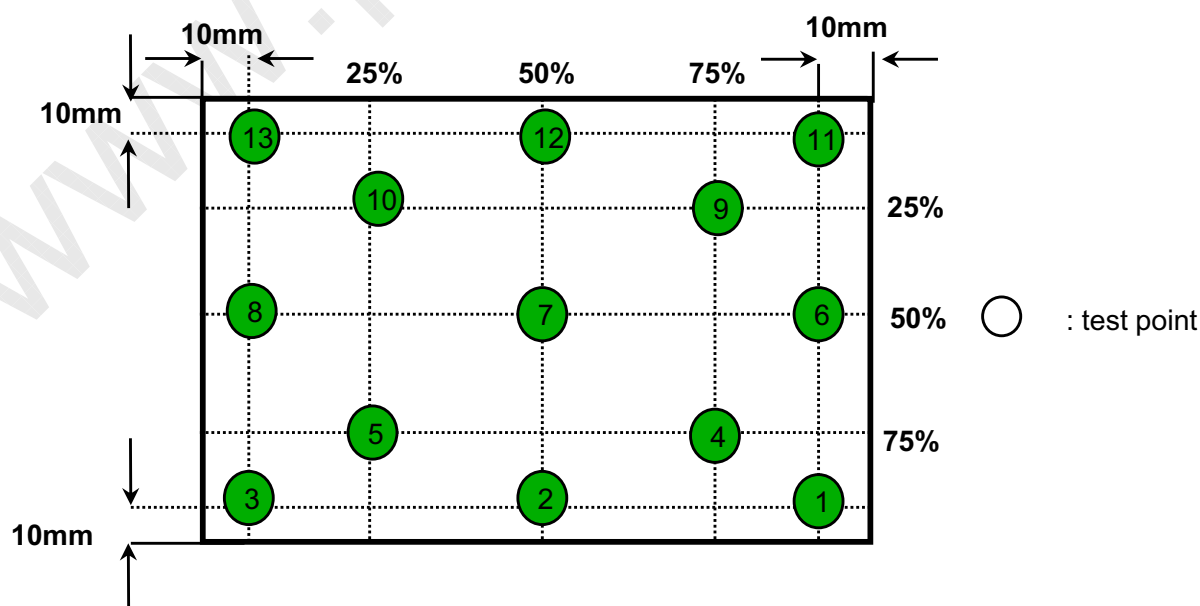
LED current : 24 mA

Environment condition : $T_a = 25 \pm 2 \text{ }^{\circ}\text{C}$



Note 6) Definition of 13 points white variation (δL), [① ~ ⑬]

$$\delta L = \frac{\text{Maximum luminance of 13 points}}{\text{Minimum luminance of 13 points}}$$



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3. ELECTRICAL CHARACTERISTICS

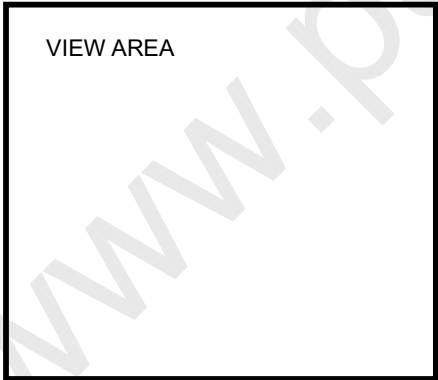
3.1 TFT LCD MODULE

Ta= 25 ± 2°C

Item		Symbol	Min.	Typ.	Max.	Unit	Note
Voltage of Power Supply		V _{DD}	3.0	3.3	3.6	V	
Differential Input Voltage for LVDS Receiver Threshold	High	V _{IH}	-	-	+100	mV	V _{CM} = +1.2V
	Low	V _{IL}	-100	-	-	mV	
Vsync Frequency		f _v	-	60	-	Hz	
Hsync Frequency		f _H	-	124.80	-	KHz	
Main Frequency		f _{DCLK}	-	138.65	-	MHz	
Rush Current		I _{RUSH}	-	-	1.5	A	(4)
Current of Power Supply	White	I _{DD}	-	700	800	mA	(2),(3)*a
	Mosaic		-	750	910	mA	(2),(3)*b

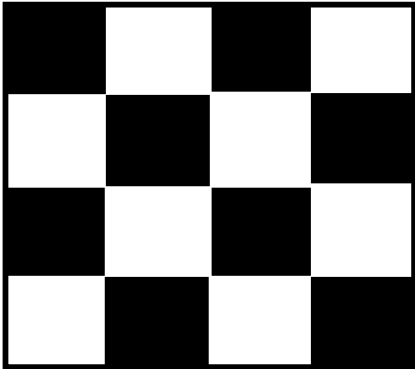
Note (1) Display data pins and timing signal pins should be connected.(GND = 0V)
(2) f_v = 60Hz, f_{DCLK} = 138.65 MHZ, V_{DD} = 3.3V , DC Current.
(3) Power dissipation pattern

*a) White Pattern



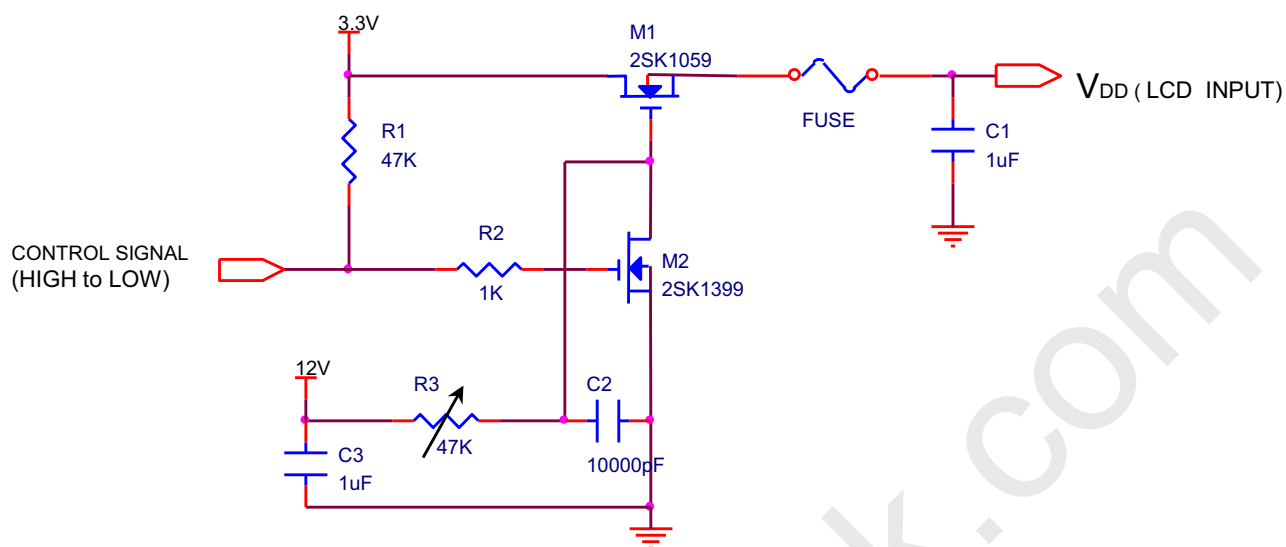
*b) Mosaic Pattern

Display Brightest Gray Level →
Display Darkest Gray Level →

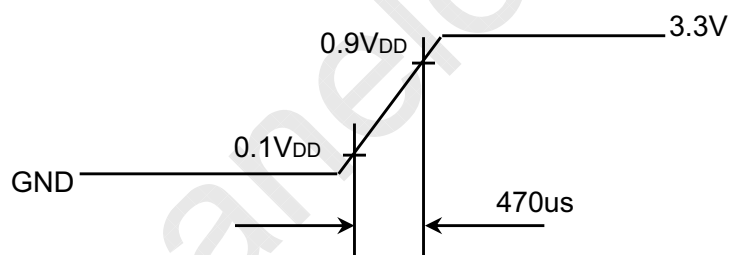


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4) Rush current measurement condition



V_{DD} rising time is 470us



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3.2 BACK-LIGHT UNIT

Ta= 25 ± 2 °C

Item	Symbol	Min.	Typ.	Max.	Unit	Note
LED Forward Current	IF	23.5	24	24.5	mA	
LED Forward Voltage	VF	3.0	3.2	3.4	V	
LED Array Voltage	VP	24	-	27.2	V	VF X 8 LEDs
Power Consumption	P	-	5.9	6.5	W	IF X VF X 64 LEDs

3.3 LED Driver

- LED Driver Manufacturer : Richtek

Ta= 25 ± 2 °C

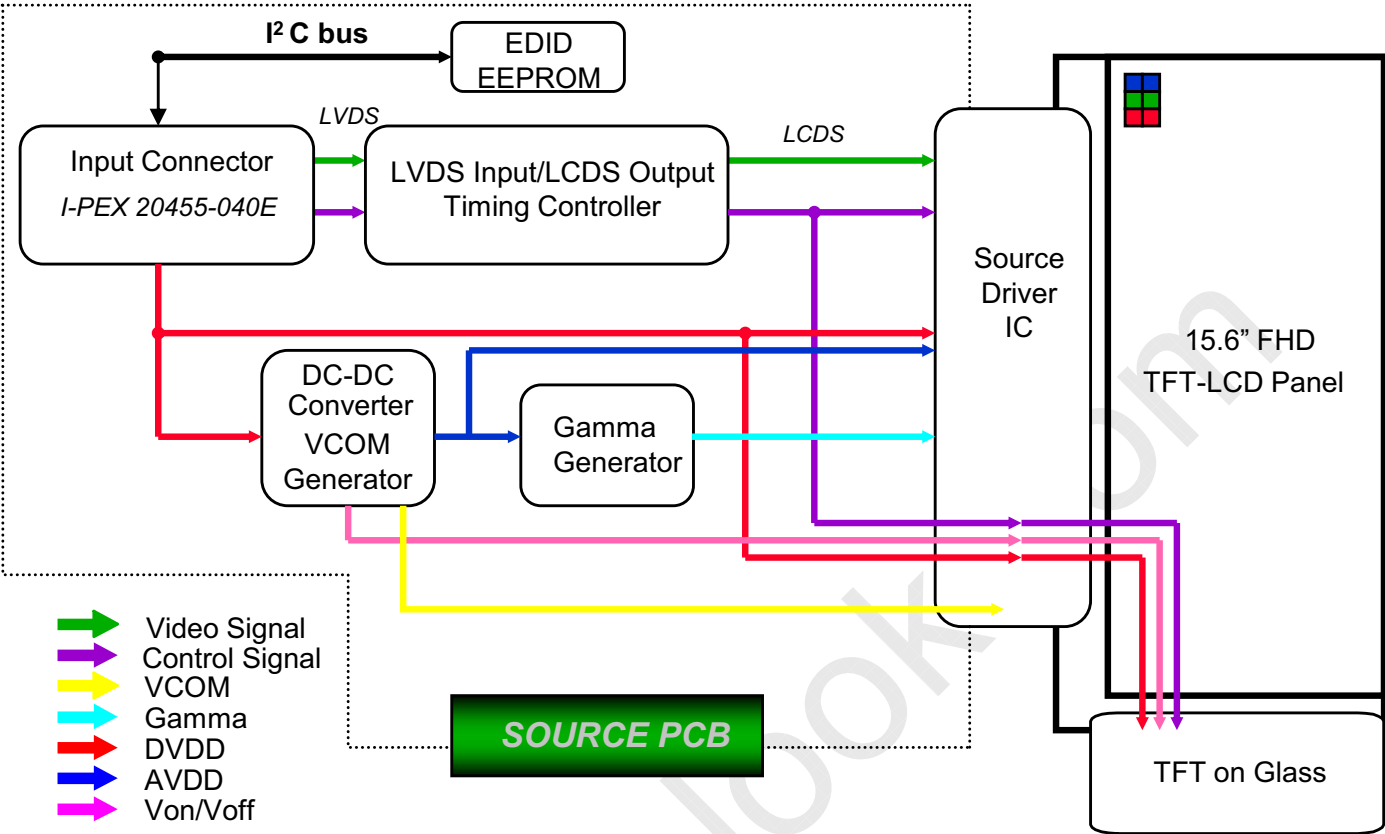
Item	Symbol	Min.	Typ.	Max.	Unit	Note
Input Voltage	V _{in}	6	-	24	V	
Output PWM Frequency	F _{PWM}	500	-	2000	kHz	No output PWM
Burst Ratio	D	5	-	100	%	PWM freq : 200Hz~1KHz
		10	-	100	%	PWM freq : 1KHz~10KHz
External PWM Dimming Control Frequency (BLIM)	F _{BLIM}	0.2	1.6	10	KHz	BLIM=PWM 0V~3.3V

Note - Test Equipment : Fluke 45

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4. BLOCK DIAGRAM

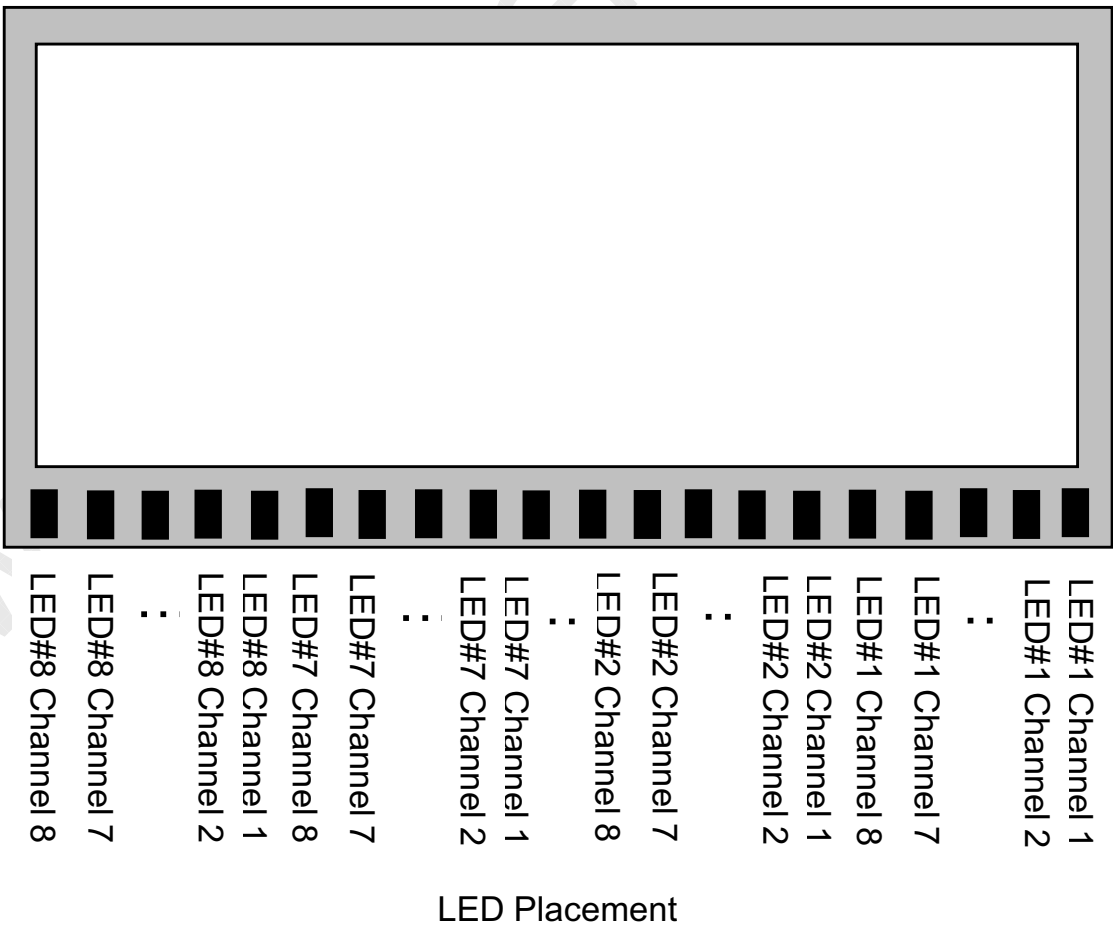
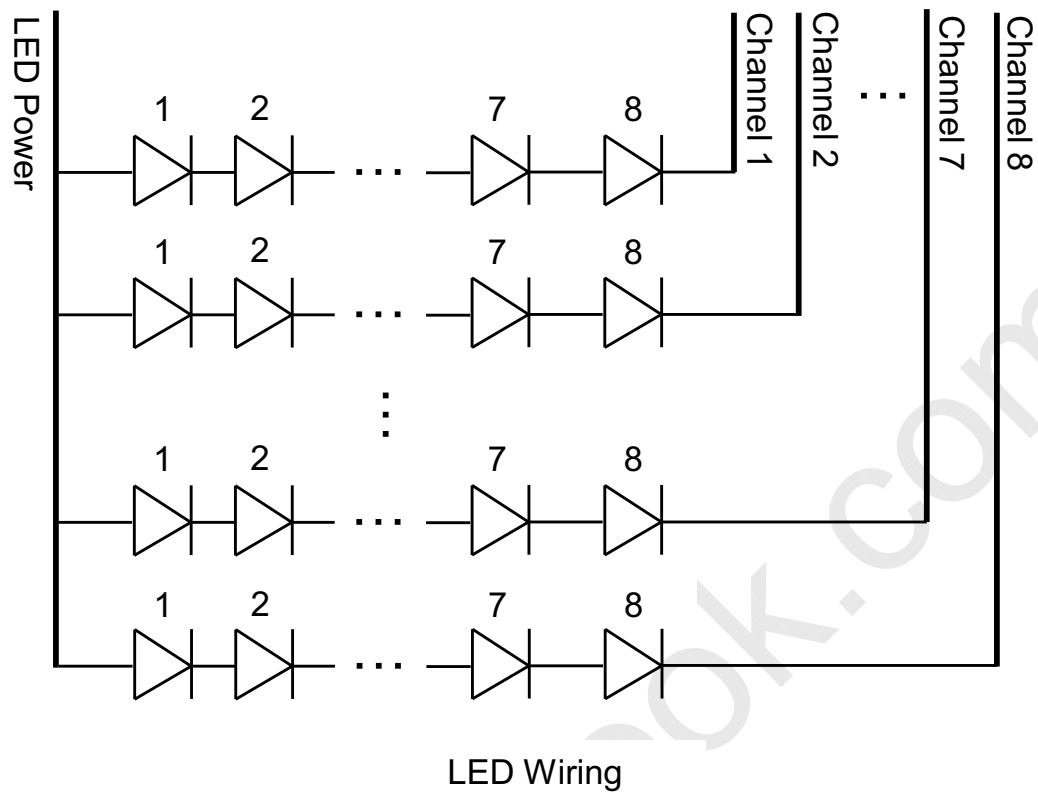
4.1 TFT LCD Module



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4. BLOCK DIAGRAM

4.2 LED connection and placement



LED Placement

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5. INPUT TERMINAL PIN ASSIGNMENT

5.1. Input Signal & Power (LVDS, Connector : I-PEX 20455-040E)

PIN #	Symbol	Description
1	NC	NC
2	VDD	Power Supply, 3.3 V (typical)
3	VDD	Power Supply, 3.3 V (typical)
4	V EEDID	DDC 3.3V power
5	TEST	Panel Self Test
6	Clk EEDID	DDC Clock
7	DATA EEDID	DDC Data
8	Odd_Rin0-	- LVDS differential data input (R0-R5, G0) (odd pixels)
9	Odd_Rin0+	+ LVDS differential data input (R0-R5, G0) (odd pixels)
10	VSS	Ground – Shield
11	Odd_Rin1-	- LVDS differential data input (G1-G5, B0-B1) (odd pixels)
12	Odd_Rin1+	+ LVDS differential data input (G1-G5, B0-B1) (odd pixels)
13	VSS	Ground – Shield
14	Odd_Rin2-	- LVDS differential data input (B2-B5, HS, VS, DE) (odd pixels)
15	Odd_Rin2+	+ LVDS differential data input (B2-B5, HS, VS, DE) (odd pixels)
16	VSS	Ground – Shield
17	Odd_ClkIN-	- LVDS differential clock input (odd pixels)
18	Odd_ClkIN+	+ LVDS differential clock input (odd pixels)
19	VSS	Ground – Shield
20	Even_Rin0-	- LVDS differential data input (R0-R5, G0) (odd pixels)
21	Even_Rin0+	+ LVDS differential data input (R0-R5, G0) (odd pixels)
22	VSS	Ground – Shield
23	Even_Rin1-	- LVDS differential data input (G1-G5, B0-B1) (odd pixels)
24	Even_Rin1+	+ LVDS differential data input (G1-G5, B0-B1) (odd pixels)
25	VSS	Ground – Shield

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5. INPUT TERMINAL PIN ASSIGNMENT

5.1. Input Signal & Power (LVDS, Connector : I-PEX 20455-040E)

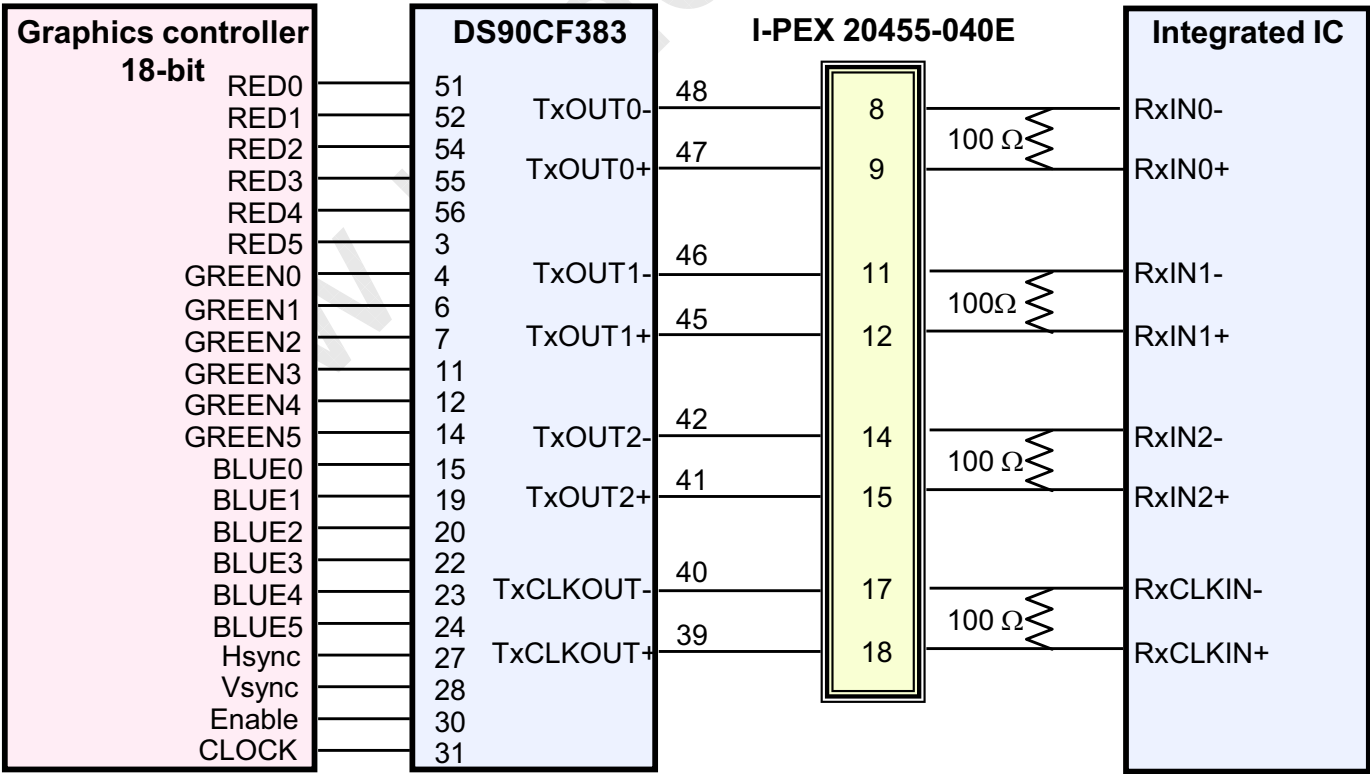
PIN #	Symbol	Description
26	Even_Rin2-	- LVDS differential data input (B2-B5, HS, VS, DE) (odd pixels)
27	Even_Rin2+	+ LVDS differential data input (B2-B5, HS, VS, DE) (odd pixels)
28	VSS	Ground – Shield
29	Even_ClkIN-	- LVDS differential clock input (odd pixels)
30	Even_ClkIN+	+ LVDS differential clock input (odd pixels)
31	VSSLED	Ground – LED
32	VSSLED	Ground – LED
33	VSSLED	Ground – LED
34	NC	NC
35	PWM	System PWM Signal Input (+3.3V Swing)
36	LED_EN	LED enable pin (+3.3V Input)
37	NC	NC
38	VDDLED	7.5V – 21V LED power
39	VDDLED	7.5V – 21V LED power
40	VDDLED	7.5V – 21V LED power

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5.2 LVDS Interface : Transmitter DS90CF363 or Compatible

Pin No.	Name	RGB Signal	Pin No.	Name	RGB Signal
51	TxIN0	R0	14	TxIN14	G5
52	TxIN1	R1	15	TxIN15	B0
54	TxIN2	R2	19	TxIN18	B1
55	TxIN3	R3	20	TxIN19	B2
56	TxIN4	R4	22	TxIN20	B3
3	TxIN6	R5	23	TxIN21	B4
4	TxIN7	G0	24	TxIN22	B5
6	TxIN8	G1	27	TxIN24	Hsync
7	TxIN9	G2	28	TxIN25	Vsync
11	TxIN12	G3	30	TxIN26	DE
12	TxIN13	G4	31	TxCLKIN	Clock

LVDS INTERFACE

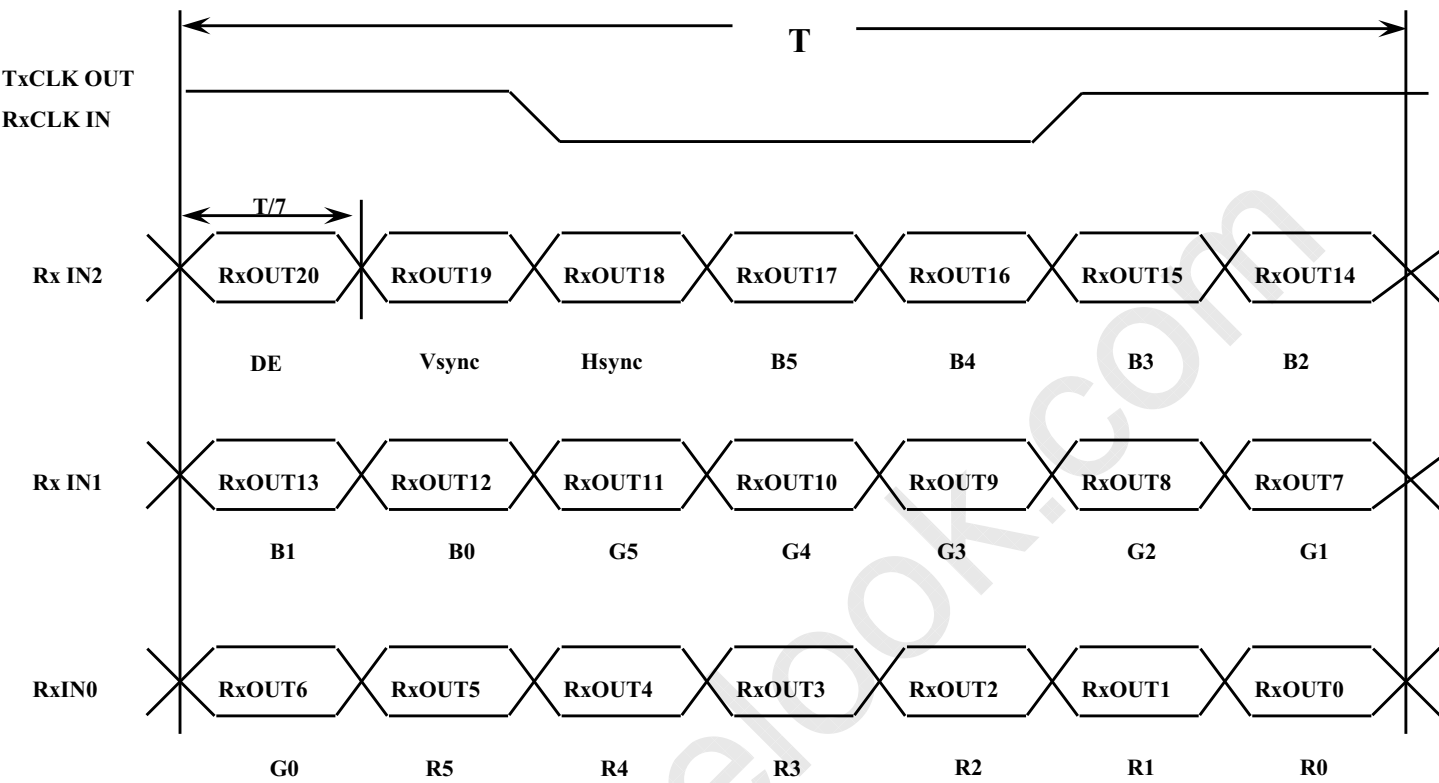


Note : The LCD Module uses a 100ohm resistor between positive and negative lines of each receiver input.

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5.3 Timing Diagrams of LVDS For Transmission

LVDS Receiver : Integrated T-CON



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5.4 Input Signals, Basic Display Colors and Gray Scale of Each Color

Color	Display	Data Signal																		Gray Scale Level
		Red						Green						Blue						
		R0	R1	R2	R3	R4	R5	G0	G1	G2	G3	G4	G5	B0	B1	B2	B3	45	B5	
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	-
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	-
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	-
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	-
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1	-
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	-
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	-
Gray Scale Of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0
	Dark	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R1
	↑	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R2
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	R3~R60
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	↓	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R61
	Light	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R62
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	R63
Gray Scale Of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	G0
	Dark	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	G1
	↑	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	G2
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	G3~G60
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	↓	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0	G61
	Light	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	G62
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	G63
Gray Scale Of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	B0
	Dark	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	B1
	↑	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	B2
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	B3~B60
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	↓	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	B61
	Light	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	B62
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	B63

Note 1) Definition of gray :

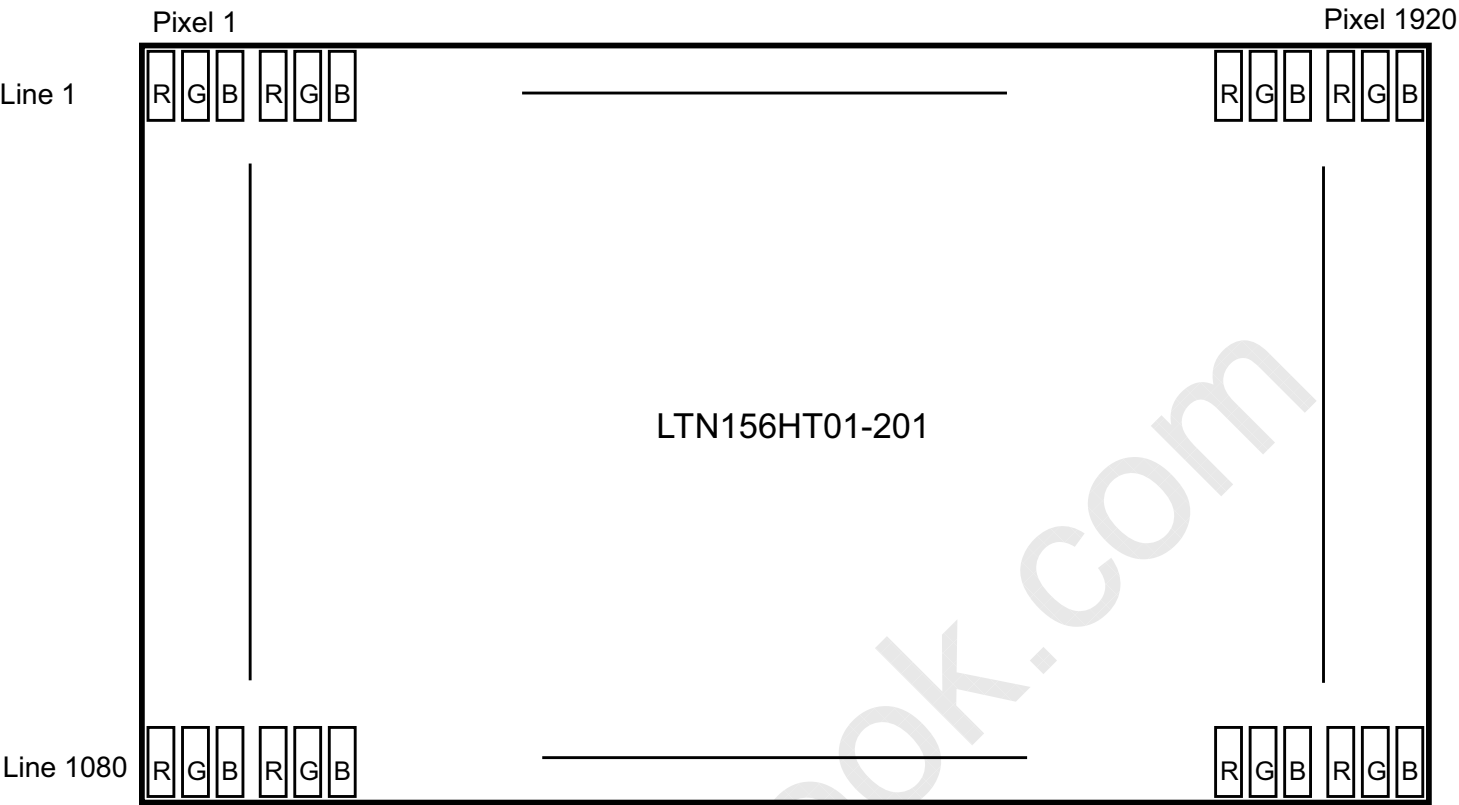
Rn: Red gray, Gn: Green gray, Bn: Blue gray (n=gray level)

Note 2)Input signal: 0 =Low level voltage, 1=High level voltage

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5.5 Pixel Format in the display



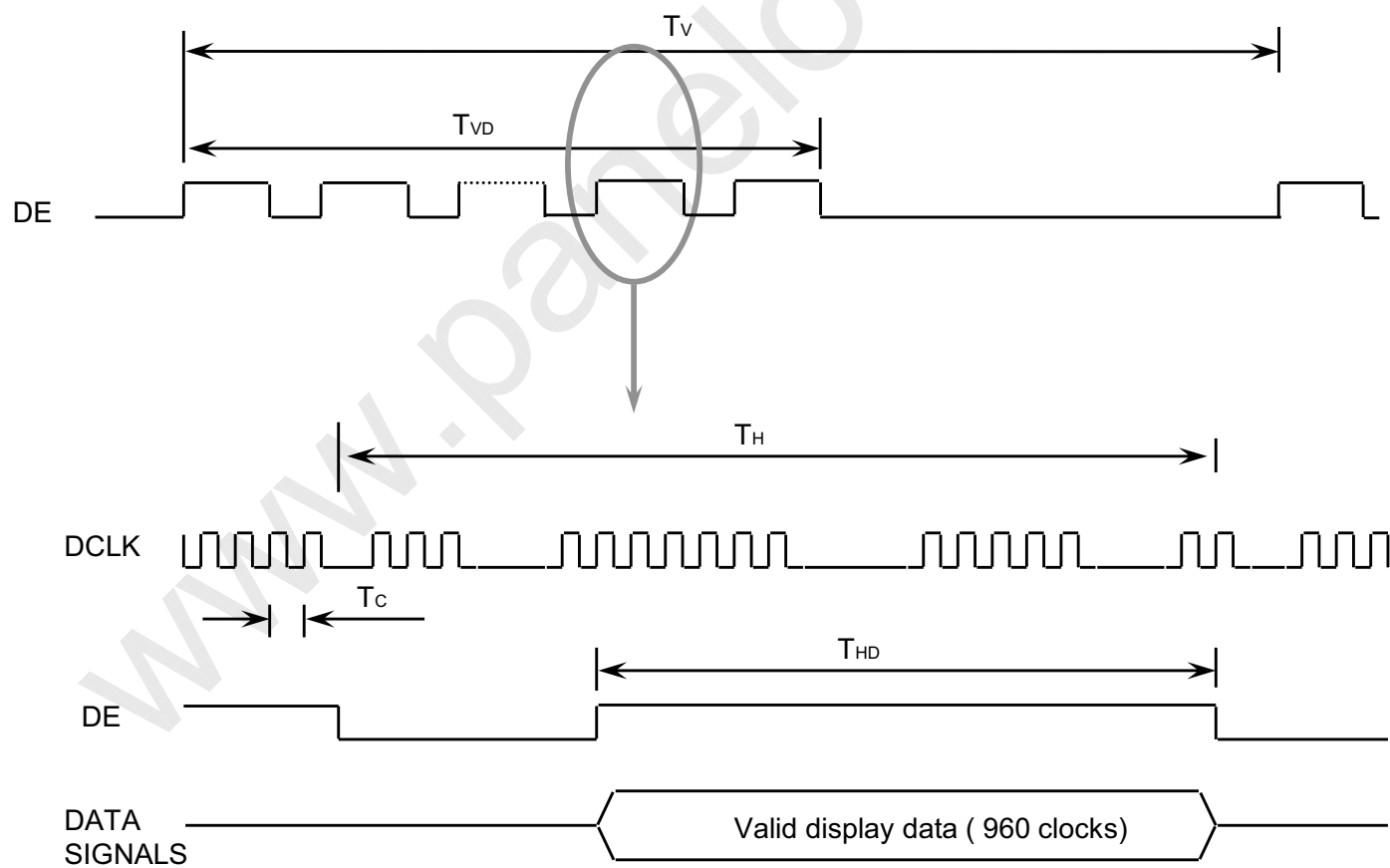
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6. INTERFACE TIMING

6.1 Timing Parameters

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
Main Clock	Frequency	1/TC	-	138.65	-	MHz	-
Frame Frequency	Cycle	TV	-	1111	-	Lines	-
Vertical Active Display Term	Display Period	TVD	-	1080	-	Lines	-
One Line Scanning Time	Cycle	TH	-	1040	-	Clocks	-
Horizontal Active Display Term	Display Period	THD	-	960	-	Clocks	-

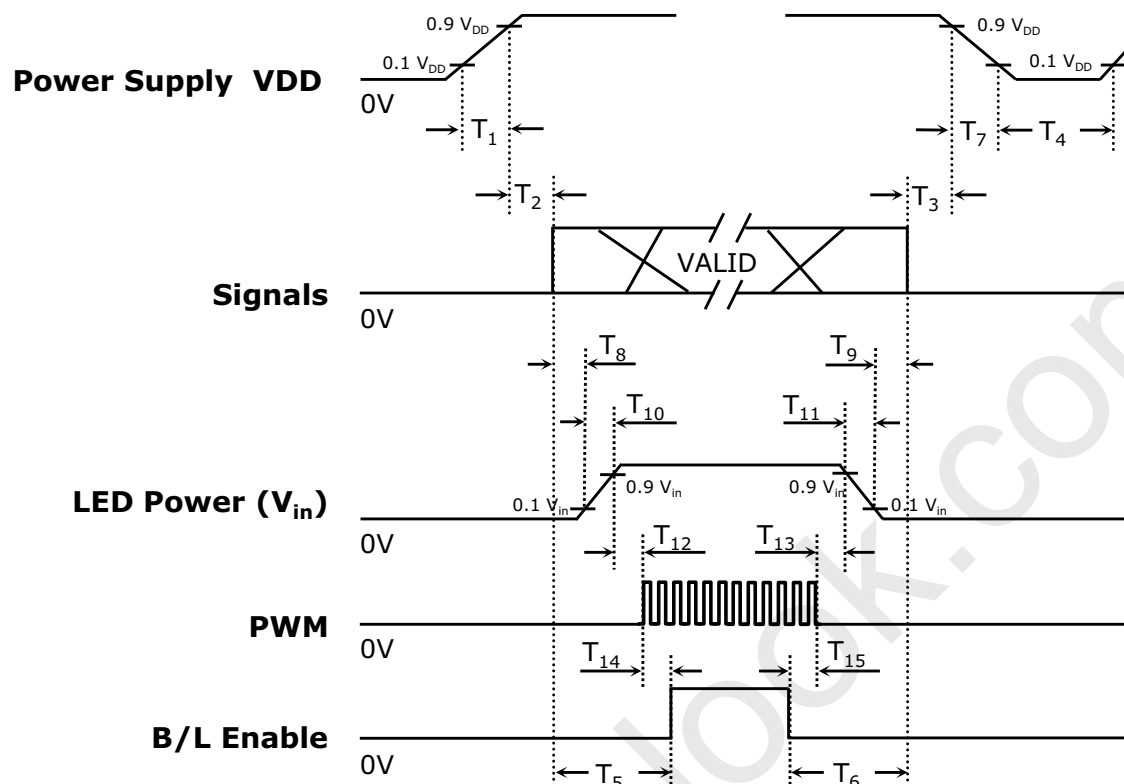
6.2 Timing diagrams of interface signal



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6.3 Power ON/OFF Sequence

: To prevent a latch-up or DC operation of the LCD module, the power on/off sequence should be as the diagram below.



Timing (ms)	Remarks
$0.5 < T_1 \leq 10$	V _{DD} rising time from 10% to 90%
$0 < T_2 \leq 50$	Delay from V _{DD} to valid data at power ON
$0 < T_3 \leq 50$	Delay from valid data OFF to V _{DD} OFF at power Off
$500 \leq T_4$	V _{DD} OFF time for Windows restart
$200 \leq T_5$	Delay from valid data to B/L enable at power ON
$200 \leq T_6$	Delay from valid data off to B/L disable at power Off
$0 < T_7 \leq 10$	V _{DD} falling time from 90% to 10%
$10 < T_8$	Delay from valid data on to LED driver V _{in} rising time 10%
$10 < T_9$	Delay from LED driver V _{in} falling time 10% to valid data Off
$0.5 < T_{10} \leq 10$	LED V _{in} rising time from 10% to 90%
$0.5 < T_{11} \leq 10$	LED V _{in} falling time from 90% to 10%
$10 < T_{12}$	Delay from LED driver V _{in} rising time 90% to PWM ON
$10 < T_{13}$	Delay from PWM Off to LED driver V _{in} falling time 10%
$10 < T_{14}$	Delay from PWM ON to B/L Enable ON
$10 < T_{15}$	Delay from B/L Enable Off to PWM Off

Note : Backlight may flash if interface signal remains floating state at invalid period.

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7. MECHANICAL OUTLINE DIMENSION

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It will be attached with PDF file

www.panelook.com

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8. PACKING

1. CARTON(Internal Package)

(1) Packing Form

Corrugated Cardboard box and Corrupad form as shock absorber

(2) Packing Method

Packing case(1SET)



PANEL 2ea / SLIT



Putting the Top Pad



Note (1) Total : Approx. 12 Kg

(2) Acceptance number of piling : 22 sets

(3) Carton size : 283(W) X 401(D) X 263(H)

(4) MAX accumulation quantity : 5 cartons

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(3) Packing Material

No	Part name	Quantity
1	Static electric protective sack	22
2	Packing case (Inner box) included shock absorber	1 set
3	Pictorial marking	2 pcs
4	Carton	1 set

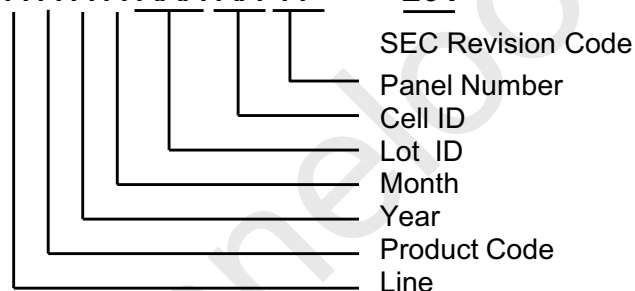
9. MARKINGS & OTHERS

A nameplate bearing followed by is affixed to a shipped product at the specified location on each product.

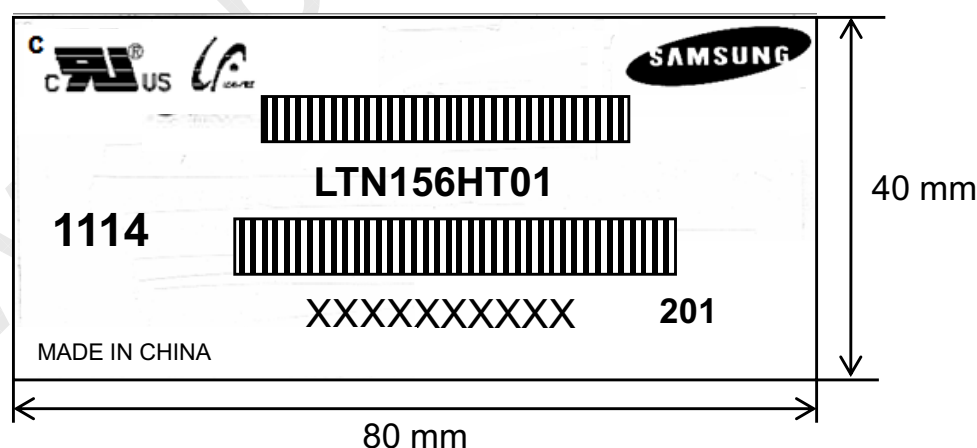
(1) Parts number : LTN156HT01-201

(2) Revision : Three letters

(3) Lot number : X X X X XXX XX X **201**



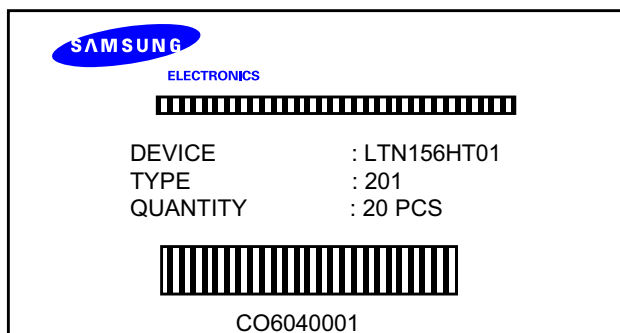
(4) Nameplate Indication(Following example is only for reference)



Parts name : LTN156HT02
 Lot number : XXXXXXXXXXXX
 Inspected work week : 1114(2011year, 14th week)
 Product revision Code : 201

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(6) Packing small box attach

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10. GENERAL PRECAUTIONS

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1. HANDLING

- (a) When the module is assembled, It should be attached to the system firmly using every mounting holes. Be careful not to twist and bend the modules.
- (b) Refrain from strong mechanical shock and / or any force to the module. In addition to damage, this may cause improper operation or damage to the module.
- (c) Note that polarizers are very fragile and could be easily damaged. Do not press or scratch the surface harder than a HB pencil lead.
- (d) Wipe off water droplets or oil immediately. If you leave the droplets for a long time, Staining and discoloration may occur.
- (e) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (f) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use Ketone type materials(ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (g) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth . In case of contact with hands, legs or clothes, it must be washed away thoroughly with soap.
- (h) Protect the module from static , it may cause damage to the C-MOS Gate Array IC.
- (i) Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (j) Do not disassemble the module.
- (k) Do not pull or fold the lamp wire.
- (l) Do not adjust the variable resistor which is located on the back side.
- (m) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (n) Pins of I/F connector shall not be touched directly with bare hands.

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2. STORAGE

- (a) Do not leave the module in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 5 to 40 °C and relative humidity of less than 70%.
- (b) Do not store the TFT-LCD module in direct sunlight.
- (c) The module shall be stored in a dark place. It is prohibited to apply sunlight or fluorescent light during the store.
- (d) Storage period is recommended not to exceed 1 year

3. OPERATION

- (a) Do not connect, disconnect the module in the “ Power On” condition.
- (b) Power supply should always be turned on/off by following item 6.3
“ Power on/off sequence “.
- (c) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.
- (d) The standard limited warranty is only applicable when the module is used for general notebook applications. If used for purposes other than as specified, SEC is not to be held reliable for the defective operations. It is strongly recommended to contact SEC to find out fitness for a particular purpose.

4. OTHERS

- (a) Ultra-violet ray filter is necessary for outdoor operation.
- (b) Avoid condensation of water. It may result in improper operation or disconnection of electrode.
- (c) Do not exceed the absolute maximum rating value. (the supply voltage variation, input voltage variation, variation in part contents and environmental temperature, so on)
Otherwise the module may be damaged.
- (d) If the module displays the same pattern continuously for a long period of time,it can be the situation when the image “sticks” to the screen.
- (e) This module has its circuitry PCB’s on the rear side and should be handled carefully in order not to be stressed.

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11. EDID

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LTN156HT01-201 EDID Sheet for ASUS

Address (HEX)	FUNCTION	Value HEX	BIN	DEC	ASCII or Data	Notes
00	Header	00	00000000	0		EDID Header
01		FF	11111111	255		
02		FF	11111111	255		
03		FF	11111111	255		
04		FF	11111111	255		
05		FF	11111111	255		
06		FF	11111111	255		
07		00	00000000	0		
08	ID Manufacturer Name	4C	01001100	76	S	3 character ID
					E	
09		A3	10100011	163	C	"SEC"
0A	ID Product Code	4C	01001100	76	[L]	48
0B		31	00110001	49	[1]	54
0C	32-bit serial no.	00	00000000	0		
0D		00	00000000	0		
0E		00	00000000	0		
0F		00	00000000	0		
10	Week of manufacture	00	00000000	0		
11	Year of manufacture	15	00010101	21	2011	2011
12	EDID Structure Ver.	01	00000001	1	1	EDID Ver. 1.0
13	EDID revision #	03	00000011	3	3	EDID Rev. 3
14	Video input definition	80	10000000	128		
15	Max H image size	22	00100010	34	34	34 cm(approx)
16	Max V image size	13	00010011	19	19	19 cm(approx)
17	Display Gamma	78	01111000	120	2.2	Gamma 2.2
18	Feature support	EA	11101010	234		
19	Red/green low bits	2D	00101101	45		
1A	Blue/white low bits	E5	11100101	229		
1B	Red x/ high bits	9D	10011101	157	0.613	
1C	Red y	5C	01011100	92	0.361	
1D	Green x	4E	01001110	78	0.308	
1E	Green y	9A	10011010	154	0.603	
1F	Blue x	27	00100111	39	0.155	
20	Blue y	1A	00011010	26	0.104	
21	White x	50	01010000	80	0.313	
22	White y	54	01010100	84	0.329	
23	Established timing 1	00	00000000	0		
24	Established timing 2	00	00000000	0		
25	Established timing 3	00	00000000	0		

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26	Standard timing #1	01	00000001	1		not used
27		01	00000001	1		
28	Standard timing #2	01	00000001	1		not used
29		01	00000001	1		
2A	Standard timing #3	01	00000001	1		not used
2B		01	00000001	1		
2C	Standard timing #4	01	00000001	1		not used
2D		01	00000001	1		
2E	Standard timing #5	01	00000001	1		not used
2F		01	00000001	1		
30	Standard timing #6	01	00000001	1		not used
31		01	00000001	1		
32	Standard timing #7	01	00000001	1		not used
33		01	00000001	1		
34	Standard timing #8	01	00000001	1		not used
35		01	00000001	1		
36	Detailed timing/monitor descriptor #1	29	00101001	41	138.65	Main clock= 138.65MHz
37		36	00110110	54		
38		80	10000000	128	1920	Hor active=1920 pixels
39		A0	10100000	160	160	Hor blanking=192 pixels
3A		70	01110000	112		4bit : 4bit
3B		38	00111000	56	1080	Vertical active=1080 lines
3C		1F	00011111	31	31	Vertical blanking=31 lines
3D		40	01000000	64		4bit : 4bit
3E		18	00011000	24	24	Hor sync. Offset = 24 pixels
3F		10	00010000	16	16	H sync. Width=16 pixels
40		25	00100101	37	2 5	V sync. Offset=2 lines V sync. Width=5 lines
41		00	00000000	0		2bit : 2bit : 2bit : 2bit
42		58	01011000	88	344	H image size= 344 mm(approx)
43		C2	11000010	194	194	V image size = 194 mm(approx)
44		10	00010000	16		
45		00	00000000	0		No Horizontal Border
46		00	00000000	0		No Vertical Border
47		19	00011001	25		
48	Detailed timing/monitor descriptor #2	00	00000000	0		Manufacturer Specified (Timing)
49		00	00000000	0		
4A		00	00000000	0		
4B		0F	00001111	15		
4C		00	00000000	0		
4D		00	00000000	0		Value=HSPWmin / 2
4E		00	00000000	0		Value=HSPWmax / 2
4F		00	00000000	0		Value=Thbpmin / 2
50		00	00000000	0		Value=Thbpmax / 2
51		00	00000000	0		Value=VSPWmin / 2
52		00	00000000	0		Value=VSPWmax / 2
53		00	00000000	0		Value=TVbpmin / 2
54		00	00000000	0		Value=TVbpmax / 2
55		28	00101000	40		Thpmin=value*2 + HA pixelclks
56		5A	01011010	90		Thpmax=value*2 + HA pixelclks
57		0A	00001010	10		Tvpmin=value*2 + VA lines
58		3C	00111100	60		Tvpmax=value*2 + VA lines
59		00	00000000	0		Module revision

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5A	Detailed timing/monitor descriptor #3	00	00000000	0		ASCII Data String Tag
5B		00	00000000	0		
5C		00	00000000	0		
5D		FE	11111110	254		
5E		00	00000000	0		
5F		53	01010011	83	[S]	
60		41	01000001	65	[A]	
61		4D	01001101	77	[M]	
62		53	01010011	83	[S]	
63		55	01010101	85	[U]	
64		4E	01001110	78	[N]	
65		47	01000111	71	[G]	
66		0A	00001010	10	[*]	
67		20	00100000	32	[]	
68		20	00100000	32	[]	
69		20	00100000	32	[]	
6A		20	00100000	32	[]	
6B		20	00100000	32	[]	
6C	Detailed timing/monitor descriptor #4	00	00000000	0		Monitor Name Tag (ASCII)
6D		00	00000000	0		
6E		00	00000000	0		
6F		FE	11111110	254		
70		00	00000000	0		
71		31	00110001	49	[1]	
72		35	00110101	53	[5]	
73		36	00110110	54	[6]	
74		48	01001000	72	[H]	
75		54	01010100	84	[T]	
76		30	00110000	48	[0]	
77		31	00110001	49	[1]	
78		2D	00101101	45	[-]	
79		32	00110010	50	[2]	
7A		30	00110000	48	[0]	
7B		31	00110001	49	[1]	
7C		0A	00001010	10	[*]	
7D		20	00100000	32	[]	
7E	Extension Flag	00	00000000	0		
7F	Checksum	4E	01001110	78		

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